

Workshop

„Memory Issues on Multi- and Manycore Platforms“

at the PPAM 2009

Background

Modern microprocessors rapidly evolve towards multi- and manycore architectures, and the respective processor performance will keep doubling every 18 months as it has done for years according to Moore's Law. However, both memory latency and memory bandwidth have not been able to keep up with this breakneck speed, nor are they likely to do so in the imminent future. As a consequence the already existing gap between processor and memory performance will keep growing.

In addition, the increasingly hybrid and hierarchical design of memory, with multi-level caches that can be exclusive to or are shared between the processor cores, as well as NUMA-style memory access will pose further roadblocks to achieving high performance on modern architectures.

Hence, in our workshop, we want to address all kinds of memory-related issues for high performance computing on multi- and manycore-based architectures. Areas of interest for workshop submissions therefore include, but are not limited to:

- Hardware-aware, compute- and memory-intensive simulations of real-world problems from electrical, mechanical, civil, or medical engineering requiring parallelisation on multicore platforms.
- Architecture-aware, and particularly multi- and manycore-aware approaches in both implementation and algorithm design, including scalability studies.
- Tools for performance and cache behavior analysis (including cache simulation) for parallel systems with multicore processors, as well as respective cache performance studies.
- Parallelization with appropriate programming models and tool support for multicore and hybrid platforms.
- Performance studies and first experiences on the latest multicore processors.

Paper Submission and Publication

[All rules of paper submission of the PPAM](#) conference apply. In particular:

- Papers will be refereed and accepted on the basis of their scientific merit and relevance to the Workshop topics.
- Papers presented at the Workshop will be included into the conference proceedings and published after the conference by [Springer](#) in the [LNCS series](#).
- Before the Workshop, abstracts of accepted papers will be posted on its WWW site.
- Authors should submit papers (PDF files) to the workshop organisers (bader@in.tum.de, trinitic@in.tum.de) before April 10, 2009. Papers are not to exceed 8 pages ([LNCS style](#)).
- Final camera-ready versions of accepted papers will be required by October 31, 2009.

Dates

Submission of Papers: **April 10, 2009**

Notification of Acceptance: May 31, 2009

Conference: September 13-16, 2009

Camera-Ready Papers: Oct 31, 2009

Session Organizers

Michael Bader, Technische Universität München, Germany

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