What is Driving Programming System Technology for Exascale and Beyond

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Collaborators and Acknowledgements

Stencils, Bricks and Geometric Multigrid
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Autotuning Search and Pragma Autotuner
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LLVM and Polly Optimization
Michael Kruse, Hal Finkel, Vinu Sreenivasan

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Which version would you prefer to write?

Code A: miniGMG baseline smooth operator approximately 13 lines of code

Code B: miniGMG optimized smooth operator approximately 170 lines of code
And now GPU code?

Code C: miniGMG optimized smooth operator for GPU, 308 lines of code for just kernel
Goal of Research

Programmer writes

Code A

Code B (CPU)

Code C (GPU)

Also, Codes D, E and F....

Programming system derives
Theme 1: Performance Portability

Can the same program perform well on diverse supercomputing platforms? (e.g., Top 500 list, top500.org)

#1: Summit, IBM Power9+V100 GPUs

#3: TaihuLight, Sunway

#4: Tianhe-2, Intel Xeon Phis

#6: Piz Daint, Intel Xeon+P100 GPUs

#8: ABCI Intel Xeon Gold And V100 GPUs
What’s Coming Next?

Fugaku (Riken), ARM + custom optimizations

Aurora, Intel Xeon + Intel X Compute

Frontier, AMD EPYC CPU + AMD GPU
Communication wall will get worse (dominates energy and time)

- Optimizing for memory/network more important than ever
- Automatic data movement (caches, VM) can be wasteful
- Autotuning (search) helps reach bandwidth limits
Stencil Computations

- Solve partial differential equations
  - Points are computed using neighbors
- Low order stencil
  - Lower accuracy
  - Low arithmetic intensity (FLOP per byte) typically memory bound
- High order stencil
  - High arithmetic intensity and could be compute bound
  - Conventional wisdom: memory optimization is not as important
- Diameter of stencil related to order of stencil
  - Low order stencil - smaller diameter
  - High order stencil - larger diameter
Data Movement Arising from Stencils

- Hardware prefetching streams
- TLB entries
- Worst case usage (cube-shaped):
  - \( \sim \) diameter in 2D
  - \( \sim \) diameter\(^2\) in 3D

Usage limits parallelism
- e.g. number of threads < streams

- Problem exacerbated with tiling
- Tiling factors are architecture specific
  - Size of cache, page size, number of prefetching stream
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![Diagram of data movement](image.png)
Approach #1: Code A to Codes B & C

• Extended compiler transformation and code generation framework with \textit{domain-specific specialization} (supports C-like C++)
  • Target is loop-based scientific applications and related tensor computations such as CNNs
  • \textit{Composable} transformations

• Optimization strategy can be specified or derived with \textit{transformation recipes}
  • Also optimization parameters exposed
  • \textit{Separates code from mapping}!

• \textit{Autotuning}
  • Systematic exploration of alternate transformation recipes and their optimization parameter values
  • Search technology to prune combinatorial space

\begin{verbatim}
for (i=0;i<N;i++) {
  for (j=1;j<M;j++) {
    S0: a[i][j] = b[j] – a[i][j-1];
    I = \{[i,j] \mid 0<=i<N \land 1<=j<=M\}
  }
\end{verbatim}
/* jacobi_box_4_64.py, 27-pt stencil, 64³ box size */
from chill import *

#select which computation to optimize
source('jacobi_box_4_64.c')
procedure('smooth_box_4_64')

loop(0)
original()  # fuse wherever possible

# create a parallel wavefront
skew([0,1,2,3,4,5],2,[2,1])
permute([2,1,3,4])

# partial sum for high order stencils and fuse result
distribute([0,1,2,3,4,5],2)

stencil_temp(0)
stencil_temp(5)
fuse([2,3,4,5,6,7,8,9],1)
fuse([2,3,4,5,6,7,8,9],2)
fuse([2,3,4,5,6,7,8,9],3)
fuse([2,3,4,5,6,7,8,9],4)

/* gsrblua, variable coefficient GSRB, 64³ box size */
init("gsrb_mod.cu", "gsrb",0,0)
dofile("cudaize.lua")  # custom commands in lua

# set up parallel decomposition, adjust via autotuning
TI=32 TJ=4 TK=64 TZ=64

tile_by_index(0, {"box","k","j","i"},{TZ,TK,TJ, TI},{l1_control="bb", l2_control="kk", l3_control="jj", l4_control="ii"},
{"bb","box","kk","k","jj","j","ii","i"})

cudaize(0, "kernel_GPU",{_temp=N*N*N*N,_beta_i=N*N*N*N,_phi=N*N*N*N},{block={"ii","jj","box"}, thread={"i","j"}},{})
vectorize(x_inner, factor), equivalent to
gradient.split(x, x, x_inner, 4);
gradient.vectorize(x_inner);
gradient.parallel(tile_index);
gradient.split(x, x_outer, x_inner, 2);
gradient.unroll(x_inner), equivalent to
gradient.unroll(x, 2);
gradient.tile(x, y, x_outer, y_outer, x_inner, y_inner, 4, 4);
gradient.reorder(y, x); // similar to transpose
gradient.split(x, x_outer, x_inner, 2)
fuse(x, y, fused)
Communication Avoiding: Sometimes Code A Beats Code B!

- miniGMG w/CHiLL
  - Fused operations
  - Communication-avoiding wavefront
  - Parallelized (OpenMP)
- Autotuning finds the best implementation for each box size
  - wavefront depth
  - nested OpenMP configuration
  - inter-thread synchronization (barrier vs. point-to-point)
- For fine grids (large arrays) CHiLL attains nearly a **4.5x speedup** over baseline

Basu et al., HiPC 2013, IPDPS 2015.
Retargetable and Performance Portable: Optimized Code A can beat Code C!

- CHiLL can obviate the need for architecture-specific programming models like CUDA
  - CUDA-CHiLL took the sequential GSRB implementation (.c) and generated CUDA that runs on NVIDIA GPUs
  - CUDA-CHiLL autotuned over the thread block sizes and is ultimately **2% faster** than the hand-optimized minigmg-cuda (Code C)
  - Adaptable to new GPU generations

Basu et al., PARCO 2017.
Brick Data Layout + Code Generator
• A brick is a 4x4x4 mini domain without a ghost zone
• Application of a stencil reaches into other bricks (affinity important)
• Implemented with contiguous storage and adjacency lists
Code A uses Brick Domain-Specific Library

- Bricks are programmed using brick library for 3D stencils
  - Creation
  - Deletion
  - Access

- Brick library handles cases when access across brick boundary
- Vector code generation is carried out by a code generator

Array

```c
float c = prev[k][j][i] * coeff[0] +
    prev[k][j][i+1] + prev[k][j][i-1] +
    prev[k][j+1][i] + prev[k][j-1][i] +
    prev[k+1][j][i] + prev[k-1][j][i]) *
    coeff[1];
next[k][j][i] = c * vel[k][j][i];
```

Brick

```c
float c = prev.elem(b,k,j,i)*coeff[0]+(prev.elem(b,k,j,i+1)+prev.elem(b,k,j,i-1)+
    prev.elem(b,k,j+1,i)+prev.elem(b,k,j-1,i)+
    prev.elem(b,k+1,j,i)+prev.elem(b,k-1,j,i))*
    coeff[1];
next.elem(b,k,j,i)=c*vel.elem(b,k,j,i);
```

The index of brick
Bricks Address Themes 1 and 2

• Performance portability
  • Automation of architecture-specific code generation
  • Same abstraction, but different low-level instructions and “vector” widths

• Data movement
  • Contiguous storage of subdomain reduces overhead of automatic data movement (prefetch, TLB, cache)
  • Adjustable brick size adapts to node architecture limits
  • Indirection to represent neighbor lists gives freedom to adapt co-located bricks to architecture
    • (Ongoing) And to adapt layout to optimize communication
Performance Results (Node)

- Bricks achieve best performance for higher-order stencils, up to 5X!
- Always profitable on P100
Roofline Performance Results

- Bricks achieve performance close to memory bandwidth limit
- 125pt stencil approaches compute limit, has non-float operations

Zhao et al., PP3HPC 2018.
Zhao et al., SC19.
More on Autotuning Research: Automating Finding Codes B and C

• Bricks
  • What brick size?
  • How many bricks per core? Per node?

• Program transformations
  • Which transformations to use?
  • Parameters to optimizations, such as tile size?

• Other things to tune
  • Pragmas, e.g., OpenMP
  • Application parameters, e.g., in a library like SuperLU
Pragma Autotuner

• Search Using Random Forest (SuRF) for autotuning search (may not involve compiler)

/* Polly example */
#pragma clang loop unroll(4)
for (int i = 0; i < n; i+=1) Statement(i);

/* OpenMP example */
#pragma omp parallel loop
for (int i = 0; i < n; i+=1) Statement(i);

#pragma omp target distribute simd
for (int i = 0; i < n; i+=1) Statement(i);

Pragma Autotuner (using SuRF)

Polyhedral compiler in LLVM
Autotuning Barriers to Adoption in HPC

• Overhead
  • Tuning search can be expensive
  • Off-line tuning expensive, programmer burden
  • Specifying search space, transformations
  • Selection and configuration of algorithms

• Scope
  • Tuning must be repeated for new execution contexts
  • Exascale resources vary during execution, platform may not be available for training
  • Economies of data scale: Learning based on a community’s code

• Other programmer concerns
  • Correctness concerns with dynamically-changing code
  • Long-term tool availability

Conclusion

• The plethora of architecture technologies will make programming future supercomputers even more of a nightmare

• Programming system technology is desperately needed to address programmer productivity
  • Separating specification from architecture mapping
  • Architecture-specific code generation
  • Autotuning

• HOW TO BUILD THIS TECHNOLOGY???
**Theme 3: Leveraging Investment in Deep Learning Compilers**

**Facebook**
Glow: A community-driven approach to AI infrastructure

**Amazon**
 NNVM Compiler

**Google**
MLIR: Multi-Level Intermediate Representation Compiler Infrastructure

2019 European LLVM Developers Meeting

**Challenges and opportunities:**
- Domain-specific
- Many frontends
- Many target architectures
- Abundant parallelism and data reuse
- Must scale to large problems

Convolutional Neural Network Forward Layer Code (in C)

for (n=0; n<N; n++) { // minibatch size
    for (k=0; k<K; k++) { // output feature map
        for (c=0; c<C; c++) { // input feature map
            for (p=0; p<P; p++) { // output height
                ij = p * u; // input height
                for (q =0; q<Q; q++) { // output width
                    ii = q * v; // input width
                    for (r=0; r<R; r++) { // filter height
                        for (s =0; s<S; s++) { // filter width
                            output_seq[n][k][p][q] +=
                                input [n][c][ij+r][ii+s] * weight[k][c][r][s];
                        }
                    }
                }
            }
        }
    }
}